REMARKS

The rejection is maintained based on the contention that the Nortel patentee simply does not know what a multiplexer is and used the term "multiplexer" repeatedly when he really meant "demultiplexing."

The only support for this proposition is the fact that the inventor also suggests that the multiplexer routes something. It is respectfully submitted that the fact that a multiplexer routes something does not mean that, in fact, it is really a demultiplexer. To the contrary, it probably can be safely surmised that both demultiplexers and multiplexers route and, therefore, the mere use of the word "route," relied upon in the office action, is not commensurate with multiplexing or demultiplexing and, therefore, is non-determinative on the issue.

One skilled in the art would certainly note that, for example, in Figure 5, there are 32 lines in (note that the ingress data 500 has 32 lines as indicated by the slash mark).

Alternatively, if the Examiner's position is correct and the item 505 is not a multiplexer, then, likewise, it is not seen how it is a demultiplexer either. The Examiner seems to contend that the device 505 simply routes data from one side to the other. If this is true, 32 input lines on the left side of the device 505 feed one of four sets of 32 bits of output lines. In such case, the device 505 neither multiplexes nor demultiplexes. In such case, it still fails to meet the claimed limitation. In other words, if all the item 505 does is route and it does not demultiplex as the inventor contended, there is certainly no basis to contend that it demultiplexes either. In other words, if we assume the inventor is wrong and it is not a multiplexer, there is no basis whatsoever to contend that it is a demultiplexer. There appear to be 32 channels in and 32 channels out to each of four different registers 510. In such case, one could argue, taking the Examiner's position, that the inventor is wrong and the device 505 is not a multiplexer, but, likewise, there is no basis to conclude that it is a demultiplexer.

In such case, all Kincaid does is take 32 bit line data in chunks and transfer it to 64 bit registers 510 by making two transfers through the device 505 in succession. In other words, under this analysis he neither multiplexes or demultiplexes, he just packs the registers with two transfers that are 64 bits.

Of course, the problem with this approach is that there is no way to get anything but multiples of the data size out. With the claimed invention, by demultiplexing, one can control the

loading of the registers in smaller granularities than the data size so that you can adjust the output. Thus, in one embodiment of the present invention, 64 bits in can be changed to 66 bits out. Without demultiplexing or multiplexing in the cited reference, the only thing that is possible is to get multiples of the original size. For example, by making two transfers to the registers, 32 bits becomes 64, but there would be no way to get 66 bits out.

Therefore, reconsideration of the rejection of claim 1 is respectfully requested and, particularly, reconsideration of the rejection of claim 7 and its dependent claims would be appropriate. Likewise, on the same basis, reconsideration of the rejection of claim 11 is respectfully requested, as is reconsideration of the rejection of claim 15.

The suggestion in paragraph 8 of the office action that Kincaid is capable of converting a 66 bit wide bus is asserted, but not supported. There is no way that Kincaid could have converted 64 to 66 bits. The material cited in Kincaid at column 2 simply says he can handle any sizes. Of course he can. If he received 66 bits in he could put out two times 66 or 132. But there is no way in Kincaid that he could have received 64 bits in and outputted 66.

Claim 7 is dependent on claim 5, which is dependent on claim 4, which is dependent on claim 3, which is dependent on claim 2, which calls for receiving data in 64 bit size. There is simply no way that Kincaid could have received 64 bits and outputted 66 without a redesign adopting the claimed invention. Therefore, reconsideration would be appropriate.

With respect to the rejection based on Walker, in Walker, the blocks are never changed in size. While they may be read out on busses that are different sizes, the blocks remain the same.

In Walker, a block is 8 words. See paragraph 134, line 3. The block generator 302 forms blocks of 8 words. Thus, plainly, the output from the generator 302, namely, BLK, are blocks of 8 words each.

The pre-code or 301 receive quads of words and their respective control flags and generates a code for each quad. See paragraph 132, lines 8-12. The quad type code indicates the block type of a block. The blocks are blocks of 8 words. See paragraph 58, lines 5 and 6. In other words, what comes into the block generator 302 are blocks and what comes out of the block generator 302 are blocks. There is nothing to indicate that the size of the blocks ever change from 8 words. In other words, the item 301, before the item 302, works on blocks and blocks are defined to be 8 words and the item 302 generates blocks which are also defined to be 8 words. The only thing that the block generator 302 does is to separate the codes from the actual blocks of data and transmit

the blocks in the line 313 and the codes on the line 314. But the data is in the form of blocks of the same size "before and after." Blocks are referred to throughout the patent application to Walker and there is nothing to indicate that the blocks are anything other than 8 words.

Whether those 8 words are outputted or inputted through busses of different size, the blocks themselves never change their size. Thus, in Walker, the blocks are written and read in the same block size. Note that a quad is simply four blocks of 8 words, each of 8 bits. See paragraph 58.

After the codes are separated from the blocks, the codes are thereafter recombined with the blocks and the frame composer 305. See paragraph 135. Note the language in paragraph 135 "the pair of quad-type codes and the control word flags corresponding to the block are fed to the 18-bit wide bus 314 to the type word generator 306." It is clear that after recombination, before separation, and before storage in the register, the application specifically talks about the blocks and never suggests that those blocks change size. The only thing that may change is the number of bits associated with the code words. Certainly, Walker talks about blocks and blocks are claimed, but Walker is reasonably clear that his blocks never change size. If the code words associated with those blocks were to change size that would be irrelevant to the claimed invention.

The Abstract explains that blocks of input data are received and that these blocks comprise packets of information words and that those packets are proceeded and followed by control words. Thus, it is plain that the frame never changes size. It is only the control words that vary. The reference simply takes quads of 8 bits or 64 bits of data, also called blocks, and appends the master transition (MT), and outputs the 66 bit frame. See paragraph 142. Thus, 64 bit frames are not converted to 66 bit frames. 64 bits of pure information words have control information of two bits appended to actually form the frame. This is different from converting a 64 bit frame to a 66 bit frame.

At a higher level, at block 302, no frame has yet been formed. All we have at that point is information words and control words. The information words and control information are separated out, processed, and the control information in the form of MT, on line 316 in Figure 8B, it is provided that the frame assembler 308 which simply packs it into the information words to form the frame.

The block size never changes. The block size is always 64 bits and it is always 64 bit information words, which means they are free of control. No frame is ever formed, accept the 66 bit frame.

Thus, the cited Walker patent application does not receive a data frame of a first size. Nor is there any multiplexing of blocks to form an output data in a frame of a second size. The frames are always 66 bits.

Therefore, reconsideration is requested.

Respectfully submitted,

Date: June 4, 2007

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